Amendments to the Text of the Specification:

The text of the specification filed on March 29, 2004 replaces the substitute specification excluding claims filed on 11/3/2008.

Attachments following last page of this Amendment (6 pages).

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims (marked version):

1. (Currently Amended) A circuit of a finite impulse response (FIR) filter comprises:
a transmission delay line configured to have at least one transmission line delay element with corresponding at least one delay-time;
an input signal coupled to an input of the transmission delay line; ~~the at least one forward transmission line delay element for time-delaying the input signal by corresponding at least one forward delay time of the at least one forward transmission line delay element;~~
a ~~first~~ termination impedance coupled to an output of the ~~forward~~ transmission delay line and ~~for~~ configured to terminate~~ing~~ the ~~forward~~ transmission delay line;
a first transconductance element coupled to the input signal and configured to multiply the input signal by a first filter coefficient and to convert the input signal to a first current;
~~at least one input of the~~ at least one second~~forward~~ transconductance element coupled to at least one corresponding output of the at least one ~~forward~~ transmission line delay element ~~for~~ and configured to multiply~~ing~~ at least one time-delayed input signal by at least one ~~forward~~ corresponding filter coefficient and to ~~for~~ convert~~ing~~ at least one multiplied time-delayed input signal to at least one ~~forward~~ second ~~-~~current;

~~the at least one forward transconductance element configured to have corresponding at least one forward transconductance;~~

~~an input of a no-delay transconductance element coupled to the input signal for multiplying the input signal by a no-delay filter coefficient and for converting the input signal to a no-delay current;~~

~~the no-delay transconductance element configured to have a no-delay transconductance;~~

an output of the first~~no-delay~~ transconductance element and at least one second corresponding output of the at least one second ~~forward~~ transconductance element coupled together to form a current summing node for summing the first current and the at least one second~~forward~~ current into a summed current;

a transimpedance element coupled to the current summing node and configured to convert the summed current to a filter output voltage signal.~~;~~

~~a feedback transmission delay line configured to have at least one feedback transmission line delay element;~~

~~the output voltage signal coupled to the at least one feedback transmission line delay element for time-delaying the output voltage signal by corresponding at least one feedback delay time of the at least one feedback transmission line delay element;~~

~~a second termination impedance coupled to an output of the feedback transmission delay line for terminating the feedback transmission delay line; at least one feedback transconductance element coupled to at least one output of the at least one feedback transmission line delay element for multiplying at least one time-delayed output signal by at least one feedback filter coefficient and converting at least one multiplied time-delayed output signal to at least one feedback current;~~

~~the at least one feedback transconductance element configured to have corresponding at least one feedback transconductance; and~~

~~at least one output of the at least one feedback transconductance element coupled together at the current summing node for summing the at least one feedback current into the summed current.~~

2. (Currently Amended) The circuit~~method~~ of claim 1 wherein the input signal is single ended or differential and the output voltage signals is~~are~~ single ended or differential.
~~Wherein the number of transmission line segments are an integer, N, with N > 1;~~

3. (Currently Amended) The circuit~~method~~ of claim 1 wherein the said transmission line ~~segments~~delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a ~~silicon or other~~ semiconductor substrates, on a~~the~~ package substrate~~,~~ or on a printed circuit ~~PCB~~ board (PCB~~,~~ ).~~as co-planar waveguides, as microstrip lines, as stripline transmission lines or any other known transmission line types.~~

4. (Currently Amended) The circuit~~method~~ of claim 1 wherein each of the said transmission line delay elements ~~segments can have its own~~ has a fixed or a programmable delay time~~value~~.

5. (Currently Amended) The circuit of claim 1 wherein ~~a number of the at least one forward~~ the transmission delay line ~~delay elements and a number of the at least one~~ comprises a fixed or programmable number of ~~feedback~~ transmission line delay elements~~.~~ ~~are fixed or programmable.~~

6. (Currently Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second~~forward~~ transconductance elements ~~and the at least one feedback transconductance element is implemented~~ is configured as a transconductance amplifier, as a multistage voltage amplifier, resistors, or a combination of resistors and voltage amplifiers.

7. (Currently Amended) The circuit of claim 1 wherein each of the first transconductances element~~of the no-delay~~ and~~,~~ the at least one ~~forward and the at least one~~ second~~feedback~~ transconductance elements is configured to have a fixed value, a programmable value, or an adaptively controlled value.

8. (Cancelled)

9. (Currently Amended) The circuit of claim 1 wherein ~~each of the first and~~ the ~~second~~ termination impedances is configured to have a matched or mismatched impedance in response to a system filter requirement specification.

10. (Currently Amended) The ~~method~~ circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for a~~has~~ fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Currently Amended) The circuit~~method~~ of claim 1 further comprises input~~wherein~~ matching impedance~~components~~ elements configured for matching to ~~are placed at~~ the corresponding inputs of the said transconductance elements.~~; wherein the impedance element comprises a resistor or resistors, capacitors, inductors or resistor, capacitor and inductor combination networks; wherein the impedance element has fixed impedance, programmable impedance, or adaptively adjustable impedance~~

12.-14. (Cancelled)

15. (Currently Amended) The circuit of claim 1 wherein the analog filter is configured as an ~~in~~finite impulse response (FIR) filter for equalizing an~~the~~ input signal in disk drives, optical , serial chip-to-chip, serial backplane high speed networks, or radio frequency communication systems.

16-30. (Cancelled)